Featured Talk: Bus Coding for Low-Power On-chip Interconnects

Wai Ho Mow

HongKong University of Science and Technology, Hong Kong, China

Abstract. Due to the recent drastic demand on AI accelerator hardware, novel very-large-scale (and even wafer-scale) circuit integration architectures, which may involve 3D stacking mutliple chiplets onto silicon interposers with sophisticated layer interconnections, have been introduced. The capacitive crosstalk of the on-chip bus interconnects induces high power consumption and limits data transmission speed. The classical solution of adding ground shielding is area-inefficient. One of the more area-efficient approaches, called bus coding, is to add one or a few redundant wires which send encoded signals in such a way that the overall latency and/or power consumption is reduced. The most famous single-redundancy-wire bus code is the bus invert code, which has been standardized and adopted in numerous inter-chip bus interconnects applications. In this talk, various known families of low-power bus codes will be surveyed. It will be pointed out that many known bus codes may actually increase, rather than decrease, overall power consumption, after the codec power consumption is taken into consideration. Lastly, our latest works on low-power bus codes, which can achieve the state-of-the-art overall power saving, will be presented.